

# REALTEK

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**RTL2832U**

**DVB-T COFDM DEMODULATOR+USB 2.0**

**DATASHEET**

**(CONFIDENTIAL: Development Partners Only)**

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## **USING THIS DOCUMENT**

This document is intended for the hardware and software engineer’s general information on the Realtek RTL2832U.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## **REVISION HISTORY**

| Revision | Release Date | Summary                                                                                                                                                                           |
|----------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.0      | 2008/06/30   | First release.                                                                                                                                                                    |
| 1.1      | 2009/02/06   | Corrected typing errors.                                                                                                                                                          |
| 1.2      | 2009/02/16   | Revised ‘Connects a 12k ohm Resistor to ground’ to ‘Connects a 10k ohm Resistor to ground’, in the ADC section of Table 1 Pin Descriptions, page 5.<br>Revised Figure 9, page 44. |
| 1.3      | 2009/06/29   | Corrected minor typing errors.                                                                                                                                                    |
| 1.4      | 2010/11/01   | Added Table 38 Crystal Conditions, page 43.                                                                                                                                       |

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## 1. General Description

The RTL2832U is a high-performance DVB-T COFDM demodulator that supports a USB 2.0 interface. The RTL2832U complies with NorDig Unified 1.0.3, D-Book 5.0, and EN300 744 (ETSI Specification). It supports 2K or 8K mode with 6, 7, and 8MHz bandwidth. Modulation parameters, e.g., code rate, and guard interval, are automatically detected.

The RTL2832U supports tuners at IF (Intermediate Frequency, 36.125MHz), low-IF (4.57MHz), or Zero-IF output using a 28.8MHz crystal. Embedded with an advanced ADC (Analog-to-Digital Converter), the RTL2832U features high stability in portable reception.

The state-of-the-art RTL2832U features Realtek proprietary algorithms (patent-pending), including superior channel estimation, co-channel interface rejection, long echo channel reception, and impulse noise cancellation, and provides an ideal solution for a wide range of applications for PC-TV, such as USB dongle and MiniCard/USB, and embedded system via USB interface.

## 2. Features

- COFDM complying with Nordig Unified 1.0.3, D-book 5.0, and ETSI 300-744
- Supports multiple IF frequencies (4.57MHz or 36.167MHz) and spectrum inversion
- Supports Zero-IF input
- Single low-cost crystal for clock generation ( $\pm 100\text{ppm}$ )
- Automatic transmission mode and guard interval detection
- Impulse noise cancellation circuits
- Automatic carrier recovery over a wide range offset ( $\pm 800\text{KHz}$ )
- Superior performance with pre/post/long echo profiles
- Embedded adjacent and co-channel interference rejection circuit
- Delayed AGC with programmable Take-Over Point (TOP)
- 7-bit ADC for RF signals level measurement
- Hardware MPEG-2 PID filters
- Infra-red port for remote control and wake-up, protocols supported are
  - ◆ Microsoft RC6 protocol
  - ◆ NEC, Sony, SIRC, RC-5 protocol
- Eight general purpose I/O ports
- USB 2.0 Interface
  - ◆ Supports USB Full/High speed
  - ◆ Configurable vendor information via external EEPROM
  - ◆ Passes USB-IF certification
- Signal 3.3V external power is required
- 48-pin QFN (6x6 mm<sup>2</sup>) Green Package

## 3. System Applications

- Portable DTV device
- USB dongle
- MiniCard

## 4. Block Diagram

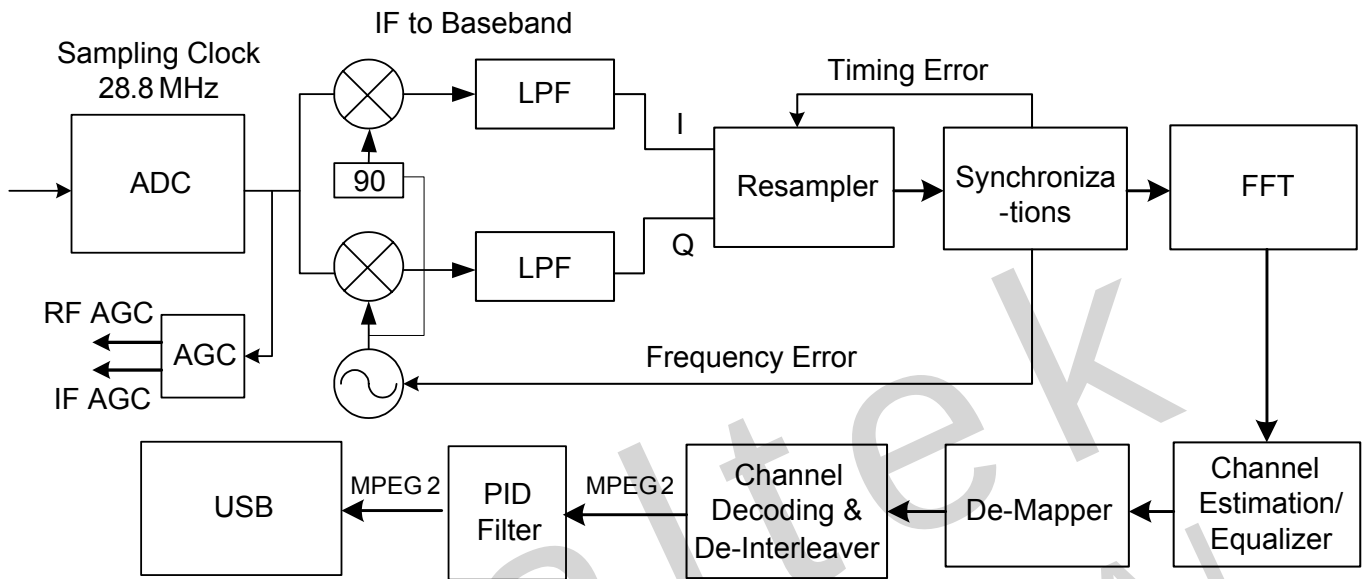


Figure 1. Block Diagram

## 5. Pin Assignments

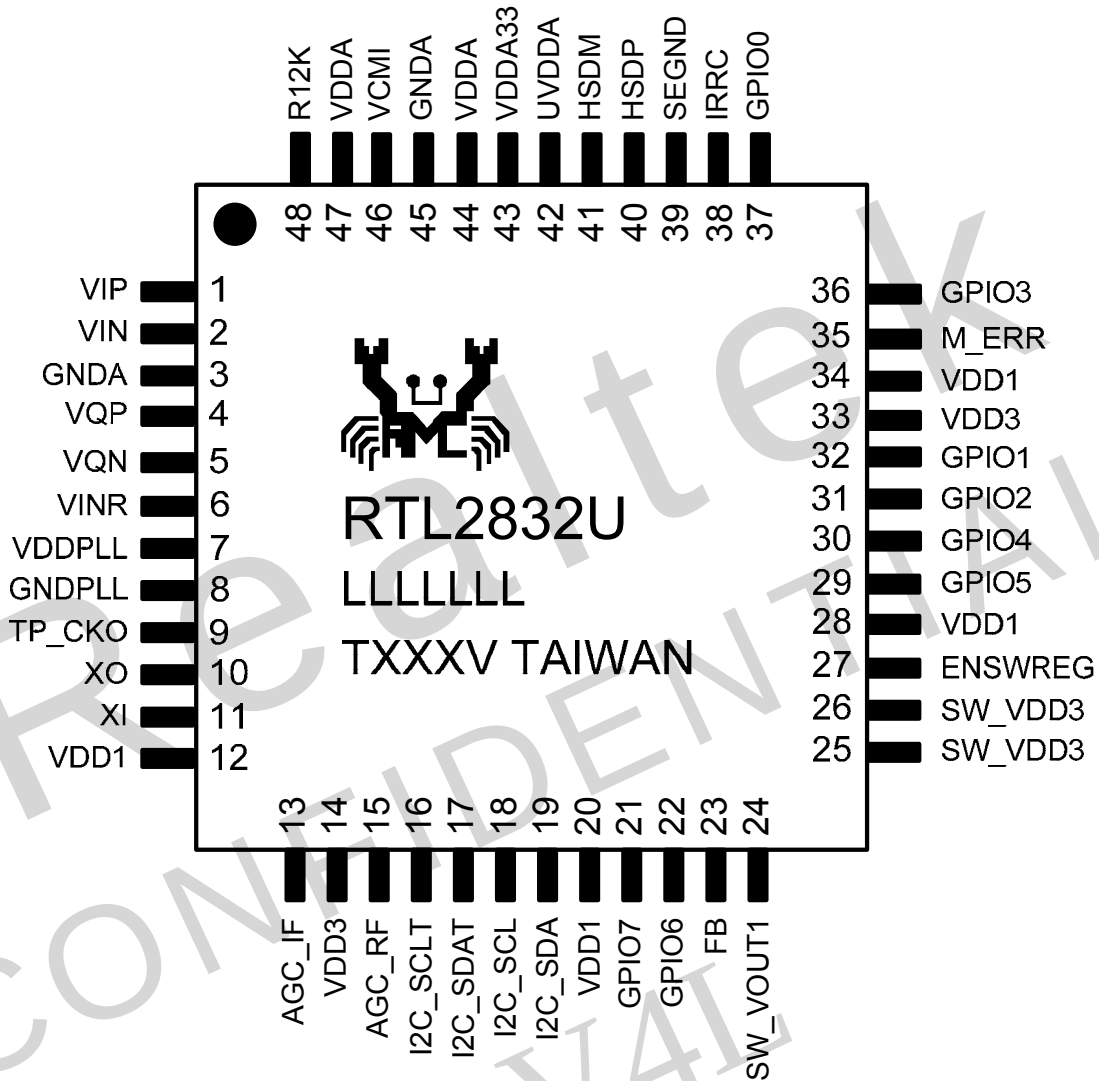


Figure 2. Pin Assignments (48-Pin QFN)

### 5.1. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. The version number is shown in the location marked 'V'.

## 6. Pin Descriptions

The following signal type codes are used in the tables:

I: Input

I/OD: Bi-Directional, Output Open-Drain

O: Output

Tri: Tri-State Output

OD: Open-Drain Output

PS: Power Supply

I/O: Bi-Directional

GND: Ground

**Table 1. Pin Descriptions**

| Name                      | Pin number     | Function                                      | Type      |
|---------------------------|----------------|-----------------------------------------------|-----------|
| <b>Power and Ground</b>   |                |                                               |           |
| VDD1                      | 12, 20, 28, 34 | Digital Core Power Supplies                   | PS (1.2V) |
| VDD3                      | 14, 33         | Digital I/O Power Supplies                    | PS (3.3V) |
| VDDA33                    | 43             | Analog Front End Power Supply                 | PS (3.3V) |
| VDDA                      | 44, 47         | Analog Front End Power Supplies               | PS (1.2V) |
| GNDA                      | 3, 45          | Analog Front End Ground                       | GND       |
| <b>Oscillator and PLL</b> |                |                                               |           |
| XI                        | 11             | Crystal Oscillator Input                      | I         |
| XO                        | 10             | Crystal Oscillator Output                     | O         |
| VDDPLL                    | 7              | PLL Power Supply                              | PS (1.2V) |
| GNDPLL                    | 8              | PLL Ground                                    | GND       |
| TP_CKO                    | 9              | ADC Test Pin for Clock Input                  | I/O       |
| <b>ADC</b>                |                |                                               |           |
| VIP                       | 1              | Differential Analog Input – Positive (I Path) | I         |
| VIN                       | 2              | Differential Analog Input – Negative (I Path) | I         |
| VQP                       | 4              | Differential Analog Input – Positive (Q Path) | I         |
| VQN                       | 5              | Differential Analog Input – negative (Q Path) | I         |
| R12K                      | 48             | Connects a 10k ohm Resistor to Ground         | I         |
| VCMI                      | 46             | Reference Voltage for ADC AC-Coupling         | I         |

| Name                                             | Pin number | Function                                                                                    | Type      |
|--------------------------------------------------|------------|---------------------------------------------------------------------------------------------|-----------|
| VINR                                             | 6          | Low Speed 7-bit ADC Single-Ended Input                                                      | I         |
| <b>USB Interface</b>                             |            |                                                                                             |           |
| HSDP                                             | 40         | USB D+ Signal                                                                               | I/O       |
| HSDM                                             | 41         | USB D- Signal                                                                               | I/O       |
| UVDDA                                            | 42         | USB 1.2V Analog Power Supply                                                                | PS (1.2V) |
| SEGND                                            | 39         | Reference Ground                                                                            | GND       |
| <b>Host Interface</b>                            |            |                                                                                             |           |
| I2C_SCL                                          | 18         | I <sup>2</sup> C Interface Clock Output Pin (5 Voltage Tolerance)                           | OD        |
| I2C_SDA                                          | 19         | I <sup>2</sup> C Interface Bi-Directional Data Pin (5 Voltage Tolerance)                    | I/OD      |
| I2C_SCLT                                         | 16         | Output SCLK Signal (5 Voltage Tolerance) for Tuner Control                                  | OD        |
| I2C_SDAT                                         | 17         | Output SDAT Signal (5 Voltage Tolerance) for Tuner Control                                  | I/OD      |
| AGC_IF                                           | 13         | Control Signal for IF AGC (5 Voltage Tolerance)                                             | OD        |
| AGC_RF                                           | 15         | Control Signal for RF AGC (5 Voltage Tolerance)                                             | OD        |
| M_ERR                                            | 35         | MPEG Error Output                                                                           | O         |
| <b>GPIO Interface and IR</b>                     |            |                                                                                             |           |
| IRRC                                             | 38         | IR Signal Input                                                                             | I         |
| GPIO[0]                                          | 37         | General Purpose I/O Pin-0                                                                   | Tri       |
| GPIO[1]                                          | 32         | General Purpose I/O Pin-1                                                                   | Tri       |
| GPIO[2]                                          | 31         | General Purpose I/O Pin-2                                                                   | Tri       |
| GPIO[3]                                          | 36         | General Purpose I/O Pin-3                                                                   | Tri       |
| GPIO[4]                                          | 30         | General Purpose I/O Pin-4                                                                   | Tri       |
| GPIO[5]                                          | 29         | General Purpose I/O Pin-5                                                                   | Tri       |
| GPIO[6]                                          | 22         | General Purpose I/O Pin-6                                                                   | Tri       |
| GPIO[7]                                          | 21         | General Purpose I/O Pin-7                                                                   | Tri       |
| <b>Internal 3.3V to 1.2V Switching Regulator</b> |            |                                                                                             |           |
| ENSWREG                                          | 27         | 0V: Turn off switching regulator<br>3.3V: Turn on switching regulator (Tie high internally) | I         |
| SW_VDD3                                          | 26, 25     | 3.3V Power Input                                                                            | PS (3.3V) |
| REG_OUT                                          | 24         | 1.2V Power Output                                                                           | O         |
| FB                                               | 23         | Regulated Feedback Voltage                                                                  | I         |

## 7. Functional Description

The block diagram of the RTL2832U DVB-T demodulator is shown in Figure 1, page 3. The RTL2832U accepts IF or Zero IF input signals with the analog signal sampled by the internal ADC. The sampled data stream is then processed by OFDM demodulation. After decoding by an on-chip FEC (Viterbi and Reed-Solomon decoder) the USB 2.0 interface outputs packets with transport stream data.

A detailed description of each block is given in this section.

### 7.1. *Analog-to-Digital Conversion (ADC)*

The internal A/D converter can accept tuner output with various bandwidths (6, 7, 8MHz), different IF frequencies (4.57M or 36.167M,), Zero IF (I & Q channel) input and can perform spectrum reversion.

Using a sampling clock generated by the internal PLL with a 28.8MHz clock source, the RTL2832U demodulates the received TV signal.

### 7.2. *Automatic Gain Control (AGC)*

The AGC circuit is used to adjust received signal strength to a moderate level for the ADC. This module supports two output paths, and both are sigma-delta modulated signals. The output signals need additional RC LPFs (Low-Pass Filters) before feeding to IF and RF VGA in the tuner. The delayed AGC algorithm is described in section 8.1 Automatic Gain Control (AGC), page 11.

### 7.3. *Digital Down Conversion*

The RTL2832U uses IF or Zero-IF sampling to process received signals. The Digital Down Conversion (DDC) circuit converts the sampled IF signal to a complex base-band signal for further processing. The down conversion frequency and low-pass filter can be programmed according to different IF frequency, sampling rates, and signal bandwidth.

## **7.4. Resampler**

The Resampler circuit changes the received signal from a fixed ADC sampling rate to an Orthogonal Frequency Division Multiplexing (OFDM) sampling rate according to the signal bandwidth. The conversion ratio can be programmed via a register setting.

## **7.5. Guard Interval Removal**

In time domain modulation, there is a guard interval inserted between two Orthogonal Frequency Division Multiplexing (OFDM) signals. It is necessary to remove the guard interval before Fast Fourier Transform (FFT) processing. This module is used to moderate the OFDM symbol boundary for FFT according to the results of synchronization.

## **7.6. Fast Fourier Transform (FFT)**

The Fast Fourier Transform (FFT) circuit converts a received time domain signal to a frequency domain signal. Based on the ETSI 300-744 definition, FFT output contains continuous pilots, scattered pilots, Transmission Parameter Signal (TPS), and data signal. These signals can be used for synchronization, channel estimation, and data decision in further processing.

## **7.7. Synchronization**

The RTL2832U can measure and compensate for a large range of sampling frequency offsets and carrier frequency offsets before making a data decision. A moderate symbol boundary is utilized to avoid Inter-Symbol Interference (ISI).

## ***7.8. Channel Estimation***

A channel estimation circuit is used to estimate the channel condition of received signals. The estimated channel response can be used for equalization, and is updated symbol by symbol to support mobile channel variations.

## ***7.9. Transmission Parameter Signal Decoder***

This module is used to decode and determine Transmission Parameter Signal (TPS) bits. The TPS carriers contain parameters for demodulation. These parameters are protected by Bose, Ray-Chaudhuri, Hocquenghem (BCH) encoding. After decoding, the RTL2832U demodulator further processes the decoded information. Parameters such as transmission mode, guard interval value, code rate etc, can be pre-set by registers to overwrite the result of TPS decoding.

## ***7.10. Equalization***

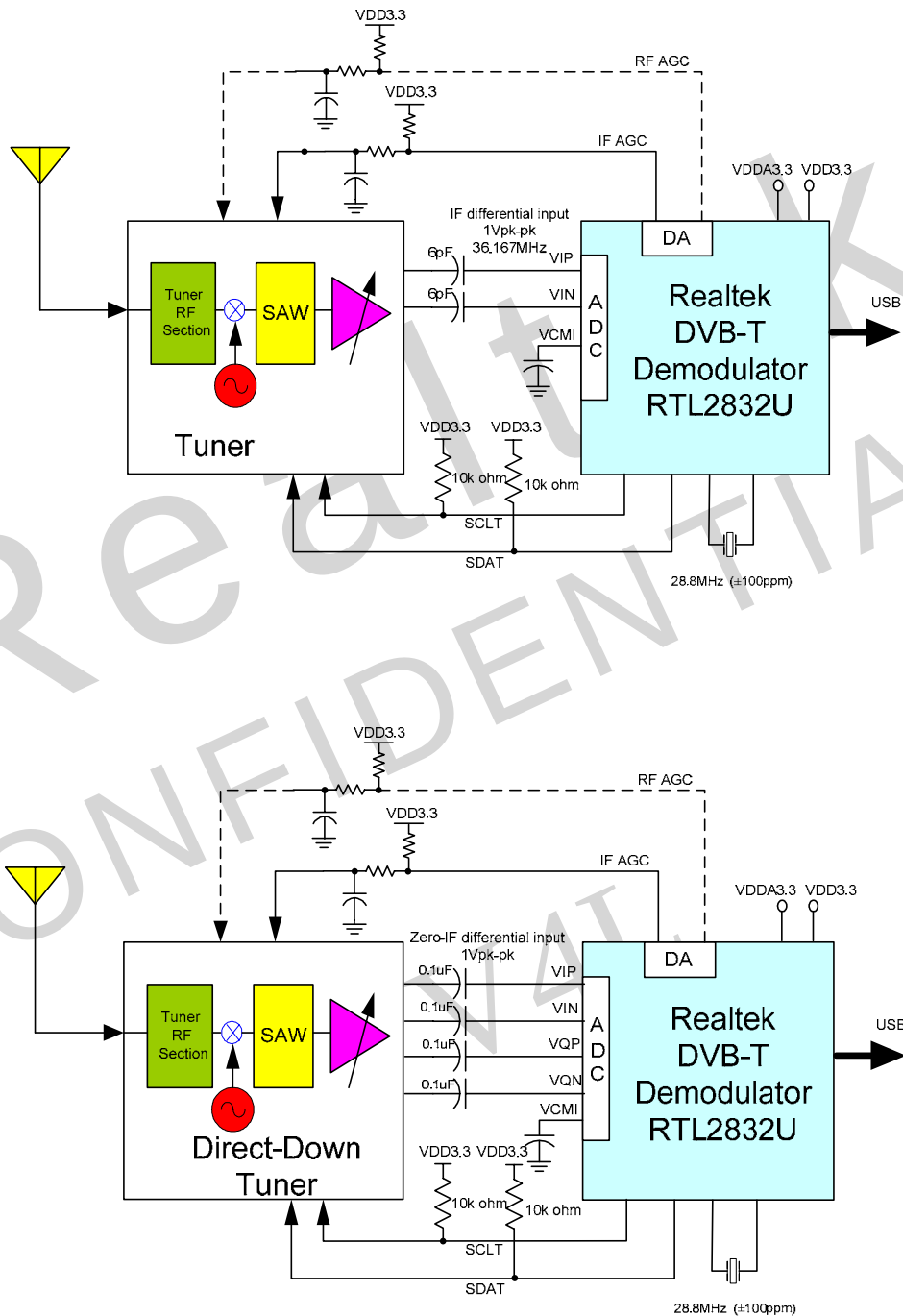
To handle various channel conditions, the equalization circuit compensates for the signal degradation caused by different multi-path channel profiles. The data bit is detected based on the equalization output.

## ***7.11. De-Interleaver, FEC Decoder, and Descrambler***

In accordance with ETSI 300-744, the RTL2832U uses a de-interleaver to re-order the decision data bit to the correct sequence. The Forward Error Correction (FEC) decoder circuit detects and corrects error bits in the received sequence. The descrambler recovers the output of the decoder to a standard Transport Stream (TS) sequence.

## 8. Tuner Interface

There are three interfaces (AGC, ADC input, two-wire serial interface) between the tuner and the demodulator.



**Figure 3. IF or Zero-IF Tuner Interface**

## 8.1. Automatic Gain Control (AGC)

In the RTL2832U, the RF\_AGC and IF\_AGC pins control the Radio Frequency (RF) and Intermediate Frequency (IF) VGA gain of the tuner. In some applications, the RTL2832U only controls IF VGA, and the tuner controls RF VGA. In some tuners, only the RF AGC is needed. The RTL2832U uses delayed AGC to control RF and IF AGC. Gain distribution for RF and IF VGA is adjusted by registers '*vtop*' and '*krf*'. The delayed AGC method is shown in Figure 4. RTL2832U has three *vtop* and four *krf* register values to be programmed by user.

When the input power of the RF tuner is weak, RF VGA gain is kept to the maximum for better tuner performance. When the input power is strong enough, RF VGA starts to decrease its gain to avoid the non-linearity effect of the following block (IF VGA). The point where RF VGA starts to decrease gain value is *vtop* (the 'take-over point'). The ratio for RF VGA gain decrease is set by register *krf*. The optimal values of registers *vtop* and *krf* depend on the tuner used.

Pins RF\_AGC and IF\_AGC are sigma-delta DAC output. An external Resistor/Capacitor (RC) low-pass filter and pull-high resistor should be placed on the PCB board to generate a quasi-DC control voltage to the tuner as shown in Figure 3, page 10.

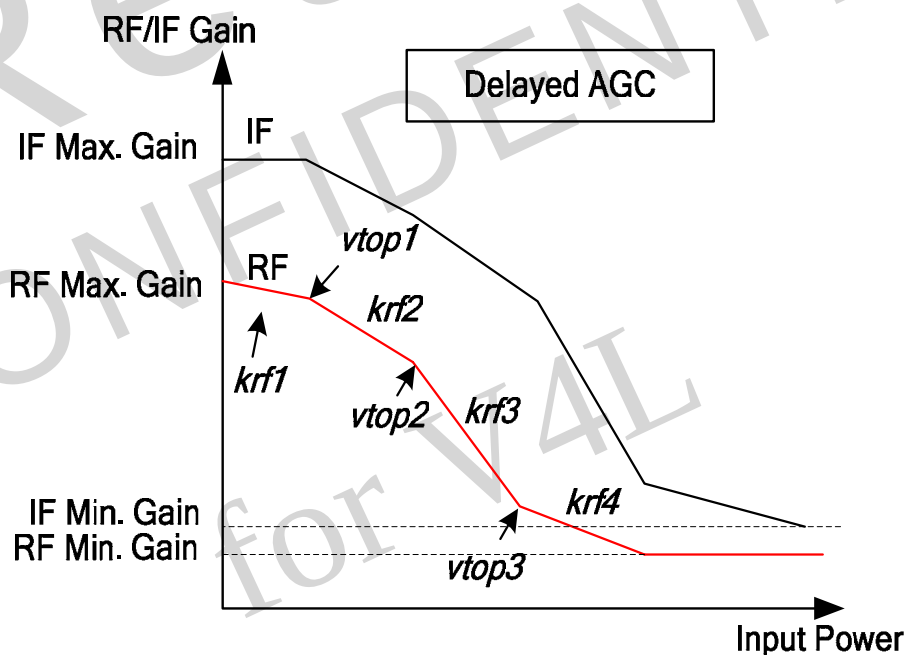


Figure 4. Delayed AGC

### 8.1.1. Register Name: loop\_gain

Analog Automatic Gain Control (AAGC) loop gain is set by register *loop\_gain2<3:0>* and *loop\_gain2<4>*. Register *loop\_gain2* can be set to 0~26. The value depends on the tuner. The recommended value is 20 (dec). A larger *loop\_gain* value would get a slower AAGC locking time, but more stable AAGC control voltage. There are another *loop\_gain1* and *loop\_gain3* for special cases: use *loop\_gain1* for aagc unlock, and use *loop\_gain3* for existing interference.

**Table 2. AAGC Register Table**

| Register Name   | Page | Offset<br>{LSB, MSB} | Bits<br>Used | RW | Default<br>(Hex) | Description                                                |
|-----------------|------|----------------------|--------------|----|------------------|------------------------------------------------------------|
| polar_rf_agc    | 0    | 0x0E                 | [1]          | RW | 0                | Inverse the AGC_RF Sigma-Delta Pin<br>0: Normal 1: Inverse |
| polar_if_agc    | 0    | 0x0E                 | [0]          | RW | 0                | Inverse the AGC_IF Sigma-Delta Pin<br>0: Normal 1: Inverse |
| loop_gain2<3:0> | 1    | 0x04                 | [4:1]        | RW | 0                | AGC Loop Gain (Bit0~Bit3) for AAGC Lock                    |
| aagc_hold       | 1    | 0x04                 | [5]          | RW | 0                | Hold AAGC Value (Open AAGC Loop)<br>0: Disable 1: Enable   |
| en_rf_agc       | 1    | 0x04                 | [6]          | RW | 1                | Enable RF AGC Loop<br>1: Enable 0: Disable                 |
| en_if_agc       | 1    | 0x04                 | [7]          | RW | 1                | Enable IF AGC Loop<br>1: Enable 0: Disable                 |
| loop_gain2<4>   | 1    | 0x05                 | [7]          | RW | 1                | AAGC Loop Gain (Bit4) for AAGC Lock                        |
| loop_gain1      | 1    | 0xC7                 | [5:1]        | RW | C                | AAGC Loop Gain for AAGC Unlock                             |
| loop_gain3      | 1    | 0xC8                 | [4:0]        | RW | 1A               | AAGC Loop Gain for Existing Interference                   |
| vtop1           | 1    | 0x06                 | [5:0]        | RW | 10               | u(6,5f) Set Take-Over Point1                               |
| vtop2           | 1    | 0xC9                 | [5:0]        | RW | 30               | u(6,5f) Set Take-Over Point2                               |
| vtop3           | 1    | 0xCA                 | [5:0]        | RW | 28               | u(6,5f) Set Take-Over Point3                               |
| krf1            | 1    | 0xCB                 | [7:0]        | RW | 2                | u(8,4f) Set RF AGC Gain Degrade Ratio1                     |
| krf2            | 1    | 0x07                 | [7:0]        | RW | F                | u(8,4f) Set RF AGC Gain Degrade Ratio2                     |
| krf3            | 1    | 0xCD                 | [7:0]        | RW | 20               | u(8,4f) Set RF AGC Gain Degrade Ratio3                     |
| krf4            | 1    | 0xCE                 | [7:0]        | RW | 30               | u(8,4f) Set RF AGC Gain Degrade Ratio4                     |
| if_agc_min      | 1    | 0x08                 | [7:0]        | RW | 80               | s(8,7f) Set IF AAGC Minimum Gain                           |

| Register Name | Page | Offset<br>{LSB, MSB} | Bits<br>Used | RW | Default<br>(Hex) | Description                      |
|---------------|------|----------------------|--------------|----|------------------|----------------------------------|
| if_agc_max    | 1    | 0x09                 | [7:0]        | RW | 7F               | s(8,7f) Set IF AAGC Maximum Gain |
| rf_agc_min    | 1    | 0x0A                 | [7:0]        | RW | 80               | s(8,7f) Set RF AAGC Minimum Gain |
| rf_agc_max    | 1    | 0x0B                 | [7:0]        | RW | 7F               | s(8,7f) Set RF AAGC Maximum Gain |
| if_agc_val    | 3    | {59,5A}              | [13:0]       | R  | -                | s(14, 13f) IF AAGC Value         |
| rf_agc_val    | 3    | {5B,5C}              | [13:0]       | R  | -                | s(14, 13f) RF AAGC Value         |
| aagc_lock     | 3    | 0x50                 | [0]          | R  | -                | AAGC Lock                        |

### 8.1.2. Register Name: if\_agc\_min/if\_agc\_max/rf\_agc\_min/rf\_agc\_max

Format: s(8,7f)

These registers limit the minimum and maximum value of RF/IF AGC. They are in 8-bit two's complement format. The maximum value 127 (dec) means maximum output voltage.

For example, if we want to limit RF minimum/maximum, AGC output voltage would be 10%/90% of pull-high voltage.

$rf\_agc\_min = \text{floor}(10\% * 255 - 128) = -103$  (dec)

$rf\_agc\_max = \text{floor}(90\% * 255 - 128) = 101$  (dec)

### 8.1.3. Register Name: Vtop

Format: u(6,6f)

The take-over point of RF VGA is set by register *vtop*. There are two special cases shown below. The optimal value depends on the tuner.

$vtop = 0$  (dec) → RF gain is always set on maximum value

$vtop = 63$  (dec) → RF gain does not delay

For example, if we want to degrade RF VGA gain when IF VGA control voltage is smaller than  $0.5 * V_{dd}$ :

$vtop = \text{floor}(63 * 0.5) = 31$  (dec)

#### 8.1.4. Register Name: *Krf*

Format: u(6,2f)

The gain degrade ratio between the RF and IF AGC when input power exceeds the RF take-over point is set by register *Krf*. A larger *krf* means the RF Gain degrade ratio is larger. This means an equal gain degrade ratio between the RF and the IF AGC. If we want RF gain to degrade quickly when input power is larger than the take-over point, *krf* should be set to a larger value. If only IF AGC is controlled by the RTL2832U, registers *vtop* and *krf* are not used.

#### 8.1.5. Register Name: *if\_agc\_val/rf\_agc\_val*

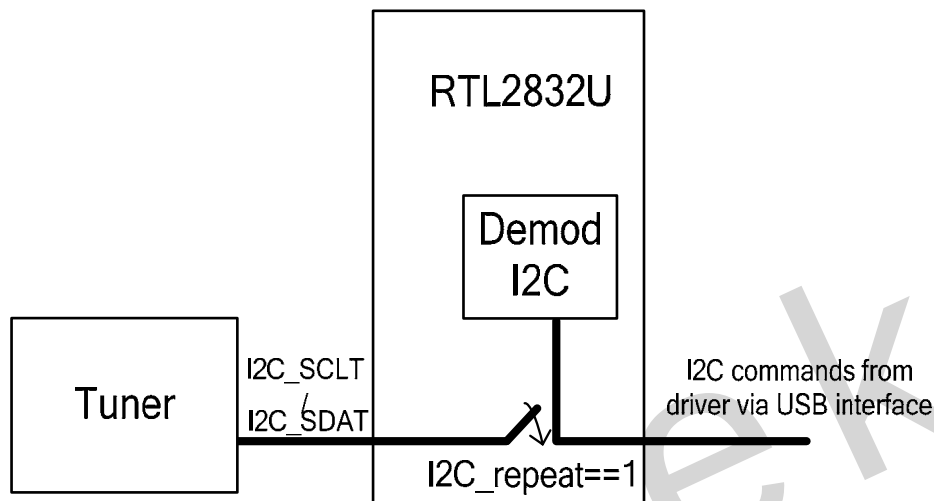
Format: s(14,13f)

The RF AAGC value and IF AAGC value are read from registers *if\_agc\_val/rf\_agc\_val*. They are in 14-bit two's complement format. The minimum value is -8192 and maximum value is 8191. When *rf/if\_agc\_val* is set to the maximum value, it means the RF/IF AGC pin output is at the maximum control voltage. The real RF input power can be mapped from *if\_agc\_val/rf\_agc\_val*. The mapping can be to a table or an equation. Note that different *vtop* and *krf* settings map different tables and equations.

### 8.2. *ADC Input (Tuner Output)*

Tuner IF or Zero IF output is AC coupled to the RTL2832U differential ADC input. An external AC coupling capacitor is required. The schematic is shown in Figure 3, page 10.

### 8.3. Two-Wire Interface Between the Tuner and the RTL2832U



**Figure 5. Two-Wire Interface between the Tuner and RTL2832U**

The RTL2832U supports an I<sup>2</sup>C repeater to prevent tuner interference from the two-wire interface. In normal situations the tuner cannot hear any command sent via the two-wire interface. We need to turn on the I<sup>2</sup>C repeater (set register *IIC\_repeat*=1) in order to send a command to the tuner. The command will be heard by the tuner and the RTL2832U at the same time. The Tuner and RTL2832U can distinguish the origin of the command by the I<sup>2</sup>C address. On the PCB, pin I2C\_SDAT/I2C\_SCLT should be connected to pull-high resistors (10k ohm) to pull-high the two-wire bus.

**Table 3. I<sup>2</sup>C Repeater Register Table**

| Register Name | Page | Offset{MSB,LSB} | Bits Used | RW | Default (Hex) | Description                                                    |
|---------------|------|-----------------|-----------|----|---------------|----------------------------------------------------------------|
| IIC_repeat    | 1    | 0x01            | [3]       | RW | 0             | I <sup>2</sup> C Repeater for Tuner<br>1: Enable<br>0: Disable |

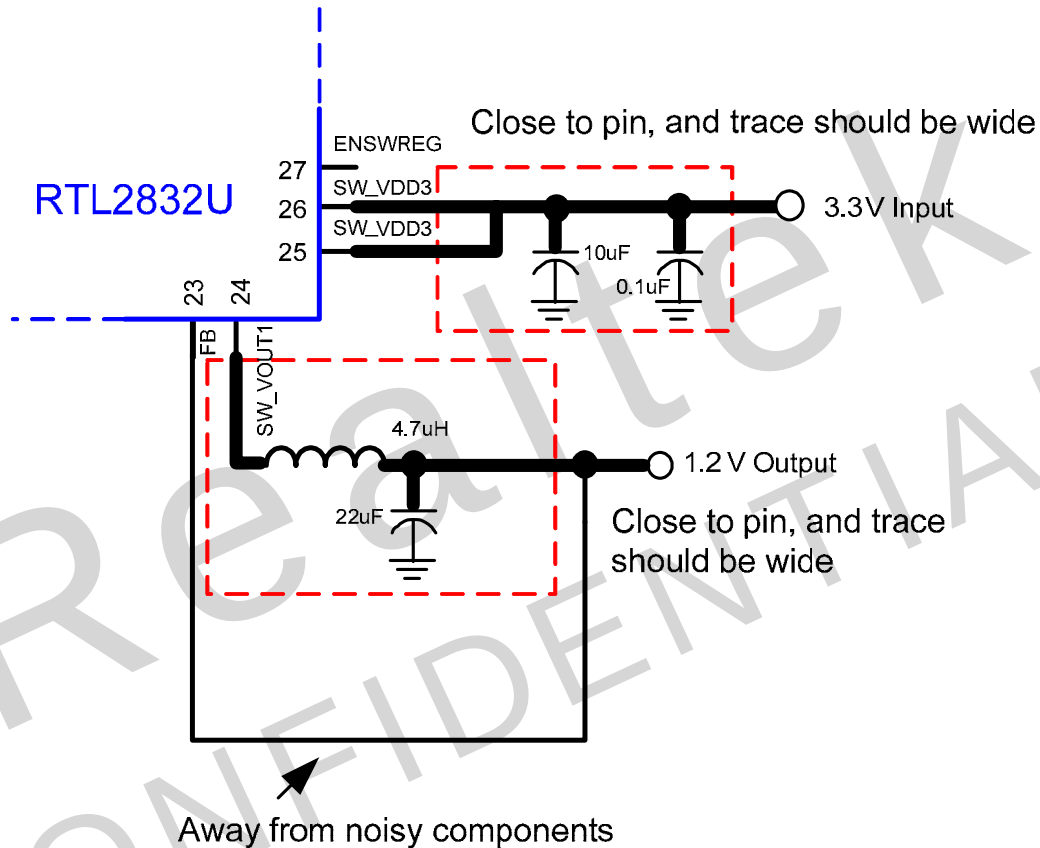
*Note 1: IIC\_repeat should be set to 1 before sending a command to the tuner.*

*Note2: IIC\_repeat is not automatically set to 0 after receiving a 'STOP' command.*

## 8.4. RTL2832U Internal Switching Regulator

The RTL2832U integrates a switching regulator with input voltage 3.3V to output voltage 1.2V. Figure 6 shows the application circuit.

The ENSWREG pin default power is 3.3V. Applying 0V turns off the switching regulator.



**Figure 6. Internal Switching Regulator Layout**

## 9. Register Descriptions (General)

### 9.1. Analog to Digital Converter (ADC)

The RTL2832U can receive IF or Zero-IF signals from the tuner. The following registers set IF or Zero-IF mode.

#### IF signal mode

- AD\_EN\_reg1 set 1
- AD\_EN\_reg0 set 0
- en\_bbin set 0

#### Zero-IF signal mode

- AD\_EN\_reg1 set 1
- AD\_EN\_reg0 set 1
- en\_bbin set 1

**Table 4. ADC Registers**

| Register Name | Page | Offset<br>{MSB,LSB} | Bits Used | RW | Default<br>(Hex) | Description                                                           |
|---------------|------|---------------------|-----------|----|------------------|-----------------------------------------------------------------------|
| AD_EN_reg1    | 0    | 0x08                | [6]       | RW | 0                | 1: Enable ADC_Q<br>0: Disable ADC_Q                                   |
| AD_EN_reg0    | 0    | 0x08                | [7]       | RW | 0                | 1: Enable ADC_I<br>0: Disable ADC_I                                   |
| en_bbin       | 1    | 0xB1                | [0]       | RW | 1                | 1: Enable Zero-IF input<br>0: Disable Zero-IF input                   |
| opt_adc_iq    | 0    | 0x06                | [5:4]     | RW | 0                | 0: Default ADC_I, ADC_Q datapath<br>1: Exchange ADC_I, ADC_Q datapath |

## 9.2. DC Cancellation and IQ Compensation

In Zero-IF mode, the output signal of the tuner often has DC bias and IQ mismatch issues. The RTL2832U will compensate for these effects. DC cancellation and IQ compensation blocks are default enabled when *en\_bbin* is set to 1.

**Table 5. DC Cancellation Registers**

| Register Name | Page | Offset {MSB,LSB} | Bits Used | RW | Default (Hex) | Description                                                                           |
|---------------|------|------------------|-----------|----|---------------|---------------------------------------------------------------------------------------|
| en_dc_est     | 1    | 0xB1             | [1]       | RW | 1             | 1: Enable DC estimation and cancellation<br>0: Disable DC estimation and cancellation |
| en_iq_comp    | 1    | 0xB1             | [3]       | RW | 1             | 1: Enable IQ compensation<br>0: Disable IQ compensation                               |
| en_iq_est     | 1    | 0xB1             | [4]       | RW | 1             | 1: Enable IQ estimation for compensation<br>0: Disable IQ estimation for compensation |
| Est_kq        | 1    | {0x66,0x67}      | [11:0]    | R  | -             | Estimated Gain for IQ Gain Mismatch, u(12,11f)                                        |
| Est_sin       | 1    | {0x68,0x69}      | [11:0]    | R  | -             | Estimated Sin for IQ $\theta$ Mismatch, s(12,10f)                                     |

### 9.3. Digital Down Conversion (DDC)

The Analog-to-Digital Converter (ADC) block sub-samples Intermediate Frequency (IF) signals, and a Digital Down Conversion (DDC) block converts the IF to baseband signals.

In normal cases, the tuner is high-side mixing and the spectrum is inversed. The demodulator requires an inverse spectrum in the DDC (register *spec\_inv*). In the RTL2832U there is an adjacent channel canceller that is enabled or disabled by register *en\_aci*. The initial IF frequency should be set by register *pset\_iffreq*. This register setting depends on the crystal frequency. The equation of *pset\_iffreq* is shown below:

$$pset\_iffreq = -\text{floor}\left(\frac{f_{IF\_D}}{f_{crystal}} \times 4194304\right)$$

Where:

$f_{IF\_D}$ : Intermediate Frequency (IF) after sub-sampling

$f_{crystal}$ : Crystal frequency

Examples:

- $f_{IF} = 4.57\text{M}$ ,  $f_{ADC} = 28.8\text{M}$ ,  
 $pset\_iffreq = -665554 \rightarrow 2^{22} - 665554 = 3528750$  (two's complement) = 0x35D82E
- $f_{IF} = 36.167\text{M}$ ,  $f_{ADC} = 28.8\text{M}$ ,  $f_{IF\_D} = 36.167 - 28.8 = 7.367$ ,  
 $pset\_iffreq = -1072897 \rightarrow 2^{22} - 1072897 = 3121407$  (two's complement) = 0x2FA0FF
- $f_{IF} = 36.125\text{M}$ ,  $f_{ADC} = 28.8\text{M}$ ,  $f_{IF\_D} = 36.167 - 28.8 = 7.367$ ,  
 $pset\_iffreq = -1066780 \rightarrow 2^{22} - 1066780 = 3127524$  (two's complement) = 0x2FB8E4
- $f_{IF} = 0\text{M}$ ,  $f_{ADC} = 28.8\text{M}$ ,  
 $pset\_iffreq = 0x0$
- DAB Mode,  
 $pset\_iffreq = -1066988 = 3127316$  (two's complement) = 0x2FB814

**Table 6. Digital Down Conversion (DDC)**

| Register Name | Page | Offset {MSB,LSB} | Bits Used | RW | Default (Hex) | Description                                                                   |
|---------------|------|------------------|-----------|----|---------------|-------------------------------------------------------------------------------|
| Spec_inv      | 1    | 0x15             | [0]       | RW | 0             | 1: Spectrum inversion<br>0: Spectrum non-inversion                            |
| En_aci        | 1    | 0x15             | [1]       | RW | 1             | 1: Enable adjacent channel rejection<br>0: Disable adjacent channel rejection |
| pset_iffreq   | 1    | {0x19,0x1B}      | [21:0]    | RW | -             | Set IF Frequency                                                              |

## 9.4. Resampler

As the ADC sampling clock is larger than the symbol ratio, there is a re-sampler to convert sampling data to symbol ratio. The ratio can be set via register ‘*rsamp\_ratio*’. The *rsamp\_ratio* is related to signal bandwidth and crystal frequency. The equation of *rsamp\_ratio* is shown below:

$$rsamp\_ratio = \text{floor}\left(\frac{f_{crystal}}{f_{symbol}} \times 4194304\right)$$

Where:

$f_{crystal}$  = crystal frequency

$f_{symbol}$  = symbol ratio of different bandwidths

- BW: 8MHz  $\rightarrow f_{symbol} = 64/7$  MHz,  $f_{crystal} = 28.8$ MHz  
 $rsamp\_ratio = 13212057$  (dec) = 0x C99999
- BW: 7MHz  $\rightarrow f_{symbol} = 8$  MHz,  $f_{crystal} = 28.8$ MHz  
 $rsamp\_ratio = 15099494$  (dec) = 0x E66666
- BW: 6MHz  $\rightarrow f_{symbol} = 48/7$  MHz,  $f_{crystal} = 28.8$ MHz  
 $rsamp\_ratio = 17616076$  (dec) = 0x 10CCCC
- DAB mode  
 $rsamp\_ratio = 14745600$  (dec) = 0x E10000

**Table 7. Resampler**

| Register Name | Page | Offset{MSB,LSB} | Bits Used | RW | Default (Hex) | Description     |
|---------------|------|-----------------|-----------|----|---------------|-----------------|
| rsamp_ratio   | 1    | {0x9F, 0xA2}    | [27:2]    | RW | C99999        | Resampler Ratio |

## 9.5. Co-Channel Interference Rejection

Narrow band in-band interference is detected and rejected by Co-Channel Interference (CCI) rejection.

Register *en\_cci* enables or disables Co-Channel Interference Rejection.

**Table 8. Co-Channel Interference Rejection**

| Register Name | Page | Offset{MSB,LSB} | Bits Used | RW | Default (Hex) | Description                                               |
|---------------|------|-----------------|-----------|----|---------------|-----------------------------------------------------------|
| En_cci        | 1    | 0x40            | [1]       | RW | 1             | 1: Enable CCI cancellation<br>0: Disable CCI cancellation |

## 9.6. Impulse Noise Cancellation

Impulse noise can be cancelled by a unique Realtek patented algorithm. Register *inc\_det\_cnt* monitors how many times impulse noise occur. Register *inc\_det\_cnt\_rst* resets the counter *inc\_det\_cnt*.

**Table 9. Impulse Noise Cancellation**

| Register Name   | Page | Offset {MSB,LSB} | Bits Used | RW | Default (Hex) | Description                                                                   |
|-----------------|------|------------------|-----------|----|---------------|-------------------------------------------------------------------------------|
| en_inc          | 1    | 0x5D             | [0]       | RW | 1             | 1: Enable impulse noise cancellation<br>0: Disable impulse noise cancellation |
| inc_det_cnt_rst | 1    | 0x5E             | [6]       | RW | 0             | Reset for inc_det_cnt<br>1: Reset<br>0: Normal                                |
| inc_det_cnt     | 3    | {0x28, 0x29}     | [8:0]     | R  | -             | Number of Impulse Noise Events                                                |

## 9.7. Digital Automatic Gain Control (DAGC)

The RTL2832U features Digital Automatic Gain Control (DAGC) to adjust optimal signal levels. DAGC can be enabled or disabled via register *en\_dagc*. The DAGC voltage gain is read from register *dagc\_val*.

Linear voltage gain of DAGC= $dagc\_val/16$ .

**Table 10. DAGC Registers**

| Register Name | Page | Offset<br>{MSB,LSB} | Bits<br>Used | RW | Default<br>(Hex) | Description                         |
|---------------|------|---------------------|--------------|----|------------------|-------------------------------------|
| en_dagc       | 1    | 0x11                | [0]          | RW | 1                | 1: Enable DAGC      0: Disable DAGC |
| dagc_val      | 3    | 0x05                | [7:0]        | R  | -                | Gain of DAGC                        |

## 9.8. FFT Mode Detection

The Fast Fourier Transform (FFT) mode and the Guard Interval are automatically detected by an auto mode detection algorithm. Auto mode detection can also be enabled or disabled by register. When auto mode detection is disabled, the correct FFT mode and Guard Interval can be set manually by register *pset\_mode\_gi*.

**Table 11. FFT Mode Detection**

| Register Name | Page | Offset<br>{MSB,LSB} | Bits<br>Used | RW | Default<br>(Hex) | Description                                                                                                                                                           |
|---------------|------|---------------------|--------------|----|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| dis_auto_scan | 1    | 0x5F                | [0]          | RW | 0                | 0: Enable auto mode detection<br>1: Disable auto mode detection                                                                                                       |
| pset_mode_gi  | 1    | 0x5F                | [3:1]        | RW | 3                | Pre-Set Guard Interval and FFT Mode<br>0: 2k, 1/32GI      1: 2k, 1/16GI<br>2: 2k, 1/8GI      3: 2k, 1/4<br>4: 8k, 1/32      5: 8k, 1/16<br>6: 8k, 1/8      7: 8k, 1/4 |
| mode_gi_idx   | 3    | 0x51                | [2:0]        | R  | -                | Mode and GI Index<br>0: 2k, 1/32GI      1: 2k, 1/16GI<br>2: 2k, 1/8GI      3: 2k, 1/4GI<br>4: 8k, 1/32GI      5: 8k, 1/16GI<br>6: 8k, 1/8GI      7: 8k, 1/4GI         |

## 9.9. Timing Recovery/Carrier Recovery

The unique synchronization algorithm in the RTL2832U is capable of dealing with tough receiving conditions. The result of sampling frequency offset can be read from the register *sfreq\_off*, which is denoted in ppm. The estimated carrier frequency offset can be read from register *cfreq\_off*, which is denoted in carrier spacing. Carrier spacing depends on signal bandwidth and transmission mode. An example of the computation is shown below:

For 8M bandwidth with 8K mode signal, the carrier spacing is approximately 1.116 KHz. If the *sfreq\_off* = 0x200 (two's complement)=512 (dec), *cfreq\_off*=0xFB2E (two's complement)=64302 (dec), then:

- Sampling frequency offset =  $sfreq\_off / 2^{24} * 1000000 = 512 / 16777216 * 1000000 = 30.5176 \text{ ppm}$
- Carrier frequency offset =  $cfreq\_off / 2^7 * \text{carrier spacing} = 64302 / 128 * 1.116 \text{ KHz} = 560.63 \text{ KHz}$

In addition, to supporting different crystal frequency sources, the register *cfreq\_off\_ratio* must be set according to the sampling frequency. The *cfreq\_off\_ratio* equation is shown below:

$$cfreq\_off\_ratio = -\text{floor}\left(\frac{f_{FFT}}{f_s} \times 1048576\right)$$

Where:

$f_{FFT}$ : FFT sampling rate

$f_s$ : ADC sampling frequency

E.g.,  $f_s = 28.8 \text{ M}$ ,  $f_{FFT} = 64/7 \text{ M}$ ,

$cfreq\_off\_ratio = -\text{floor}(64/7/28.8 * 1048576) = -332881 \text{ (dec)} = 0xAEBAF \text{ (two's complement)}$

- 8M mode,  $f_{FFT} = 64/7 \text{ M}$ :  $cfreq\_off\_ratio = 715695 \text{ (dec)} = 0xAEBAF$
- 7M mode,  $f_{FFT} = 8 \text{ M}$ :  $cfreq\_off\_ratio = 757305 \text{ (dec)} = 0xB8E39$
- 6M mode,  $f_{FFT} = 48/7 \text{ M}$ :  $cfreq\_off\_ratio = 798916 \text{ (dec)} = 0xC30C4$

### Carrier Spacing

- 8M mode,  $f_{FFT} = 64/7 \text{ M}$ :  $\text{carrier spacing (8k)} = f_{FFT} / 8192 = 1.116071 \text{ Hz}$   
 $\text{carrier spacing (2k)} = f_{FFT} / 2048 = 4.464285 \text{ Hz}$

**Table 12. Timing Recovery/Carrier Recovery**

| Register Name   | Page | Offset<br>{MSB,LSB} | Bit<br>Used | RW | Type       | Default<br>(Hex) | Description                         |
|-----------------|------|---------------------|-------------|----|------------|------------------|-------------------------------------|
| cfreq_off_ratio | 1    | {0x9D, 0x9F}        | [23:4]      | RW | s(20, 31f) | AEBAF            | Set Carrier Frequency Offset Ratio  |
| cfreq_off       | 3    | {0x5F, 0x61}        | [17:0]      | R  | s(18, 7f)  | -                | Estimated Carrier Frequency Offset  |
| sfreq_off       | 3    | {0x18, 0x19}        | [13:0]      | R  | s(14, 24f) | -                | Estimated Sampling Frequency Offset |

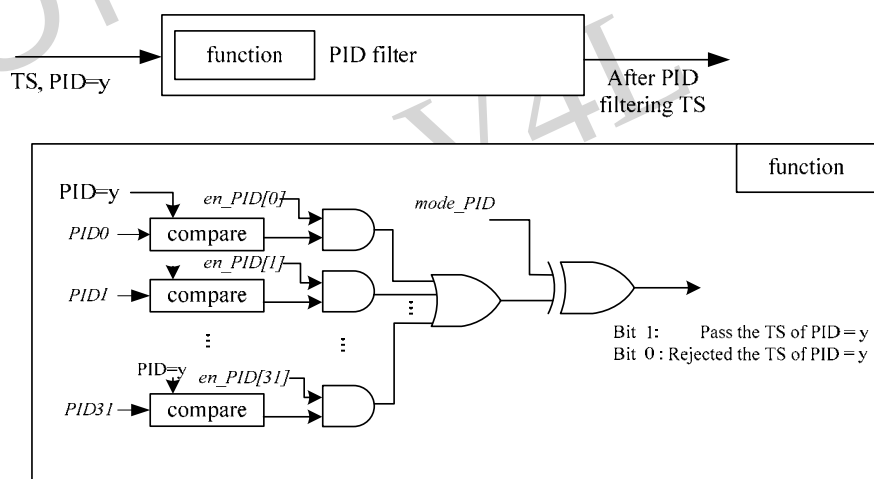
## 9.10. Crystal

The RTL2832U has superior timing offset tracking ability, allowing the use of a low-cost crystal as clock source. The timing offset tolerance is  $\pm 100$  ppm. The RTL2832U also supports an oscillator (oscillator output should be connected to the XI pin).

*Note: For different crystal frequencies, registers such as rsamp\_ratio, cfreq\_off\_ratio, and pset\_iffreq need to be set accordingly.*

## 9.11. PID Filter

A PID (Packet Identifier) filtering capability allows the reduction of the transport stream at the output of the demodulator. There are 32 PIDs that can be selected within the received multiplex. The following block diagram shows the PID filter functions, and the default register setting will let all PID transport streams pass through.


**Figure 7. PID Filter Function of the RTL2832U**

**Table 13. PID Filter**

| Register Name | Page | Offset<br>{MSB,LSB} | Bit<br>Used | RW | Default<br>(Hex) | Description                                                          |
|---------------|------|---------------------|-------------|----|------------------|----------------------------------------------------------------------|
| err_pass      | 0    | 0x61                | [5]         | RW | 1                | Set 0 to Reject All Error Packets<br>Set 1 to Pass All Error Packets |
| mode_PID      | 0    | 0x61                | [6]         | RW | 1                | Set 0 to Pass Matched PID<br>Set 1 to Reject Matched PID             |
| enable_PID    | 0    | 0x61                | [7]         | RW | 1                | Set 1 to Enable Output of PID Filter<br>Set 0 No Output              |
| en_PID[7:0]   | 0    | 0x62                | [7:0]       | RW | 0                | Enable (1) and Disable (0) Individual PID<br>Filter 0~7              |
| en_PID[15:8]  | 0    | 0x63                | [7:0]       | RW | 0                | Enable (1) and Disable (0) Individual PID<br>Filter 8~15             |
| en_PID[23:16] | 0    | 0x64                | [7:0]       | RW | 0                | Enable (1) and Disable (0) Individual PID<br>Filter 16~23            |
| en_PID[31:24] | 0    | 0x65                | [7:0]       | RW | 0                | Enable (1) and Disable (0) Individual PID<br>Filter 24~31            |
| PID0          | 0    | {0x66, 0x67}        | [12:0]      | RW | 00               | PID Value for PID Filter #0                                          |
| PID1          | 0    | {0x68, 0x69}        | [12:0]      | RW | 01               | PID Value for PID Filter #1                                          |
| PID2          | 0    | {0x6A, 0x6B}        | [12:0]      | RW | 06               | PID Value for PID Filter #2                                          |
| PID3          | 0    | {0x6C, 0x6D}        | [12:0]      | RW | 11               | PID Value for PID Filter #3                                          |
| PID4          | 0    | {0x6E, 0x6F}        | [12:0]      | RW | 12               | PID Value for PID Filter #4                                          |
| PID5          | 0    | {0x70, 0x71}        | [12:0]      | RW | 13               | PID Value for PID Filter #5                                          |
| PID6          | 0    | {0x72, 0x73}        | [12:0]      | RW | 14               | PID Value for PID Filter #6                                          |
| PID7          | 0    | {0x74, 0x75}        | [12:0]      | RW | 15               | PID Value for PID Filter #7                                          |
| PID8          | 0    | {0x76, 0x77}        | [12:0]      | RW | 16               | PID Value for PID Filter #8                                          |
| PID9          | 0    | {0x78, 0x79}        | [12:0]      | RW | 17               | PID Value for PID Filter #9                                          |
| PID10         | 0    | {0x7A, 0x7B}        | [12:0]      | RW | 18               | PID Value for PID Filter #10                                         |
| PID11         | 0    | {0x7C, 0x7D}        | [12:0]      | RW | 19               | PID Value for PID Filter #11                                         |
| PID12         | 0    | {0x7E, 0x7F}        | [12:0]      | RW | 1A               | PID Value for PID Filter #12                                         |
| PID13         | 0    | {0x80, 0x81}        | [12:0]      | RW | 1B               | PID Value for PID Filter #13                                         |
| PID14         | 0    | {0x82, 0x83}        | [12:0]      | RW | 1C               | PID Value for PID Filter #14                                         |

| Register Name | Page | Offset<br>{MSB,LSB} | Bit<br>Used | RW | Default<br>(Hex) | Description                  |
|---------------|------|---------------------|-------------|----|------------------|------------------------------|
| PID15         | 0    | {0x84, 0x85}        | [12:0]      | RW | 1D               | PID Value for PID Filter #15 |
| PID16         | 0    | {0x86, 0x87}        | [12:0]      | RW | 1E               | PID Value for PID Filter #16 |
| PID17         | 0    | {0x88, 0x89}        | [12:0]      | RW | 1F               | PID Value for PID Filter #17 |
| PID18         | 0    | {0x8A, 0x8B}        | [12:0]      | RW | 20               | PID Value for PID Filter #18 |
| PID19         | 0    | {0x8C, 0x8D}        | [12:0]      | RW | 21               | PID Value for PID Filter #19 |
| PID20         | 0    | {0x8E, 0x8F}        | [12:0]      | RW | 22               | PID Value for PID Filter #20 |
| PID21         | 0    | {0x90, 0x91}        | [12:0]      | RW | 23               | PID Value for PID Filter #21 |
| PID22         | 0    | {0x92, 0x93}        | [12:0]      | RW | 24               | PID Value for PID Filter #22 |
| PID23         | 0    | {0x94, 0x95}        | [12:0]      | RW | 25               | PID Value for PID Filter #23 |
| PID24         | 0    | {0x96, 0x97}        | [12:0]      | RW | 26               | PID Value for PID Filter #24 |
| PID25         | 0    | {0x98, 0x99}        | [12:0]      | RW | 27               | PID Value for PID Filter #25 |
| PID26         | 0    | {0x9A, 0x9B}        | [12:0]      | RW | 28               | PID Value for PID Filter #26 |
| PID27         | 0    | {0x9C, 0x9D}        | [12:0]      | RW | 29               | PID Value for PID Filter #27 |
| PID28         | 0    | {0x9E, 0x9F}        | [12:0]      | RW | 2A               | PID Value for PID Filter #28 |
| PID29         | 0    | {0xA0, 0xA1}        | [12:0]      | RW | 2B               | PID Value for PID Filter #29 |
| PID30         | 0    | {0xA2, 0xA3}        | [12:0]      | RW | 2C               | PID Value for PID Filter #30 |
| PID31         | 0    | {0xA4, 0xA5}        | [12:0]      | RW | 2D               | PID Value for PID Filter #31 |

## 10. Register Descriptions (8051 System)

The address is defined by offset value with base address 0x3000.

**Table 14. System Register Descriptions**

| Address Offset        | Access | Name             | Description                                                                                                                                                                             |
|-----------------------|--------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0000h                 | RW     | DEMOD_CTL        | Control Register for DVB-T Demodulator                                                                                                                                                  |
| <b>GPIO Registers</b> |        |                  |                                                                                                                                                                                         |
| 0001h                 | RW     | GPO              | Output Value of General Purpose I/O                                                                                                                                                     |
| 0002h                 | R      | GPI              | Input Value of General Purpose I/O                                                                                                                                                      |
| 0003h                 | RW     | GPOE             | Output Enable of General Purpose I/O                                                                                                                                                    |
| 0004h                 | RW     | GPD              | Direction Control for General Purpose I/O                                                                                                                                               |
| 0005h                 | RW     | SYSINTE          | System Interrupt Enable Register                                                                                                                                                        |
| 0006h                 | RW     | SYSINTS          | System Interrupt Status Register                                                                                                                                                        |
| 0007h                 | RW     | GP_CFG0          | PAD Configuration for GPIO0~GPIO3                                                                                                                                                       |
| 0008h                 | RW     | GP_CFG1          | PAD Configuration for GPIO4                                                                                                                                                             |
| 0009h                 | RW     | SYSINTE_1        | System Interrupt Enable Register GPIO5~GPIO7                                                                                                                                            |
| 000Ah                 | RW     | SYSINTS_1        | System Interrupt Status Register GPIO5~GPIO7                                                                                                                                            |
| 000Bh                 | RW     | DEMOD_CTL_1      | Enable IR Remote Wakeup & Low Current XTL Mode when Suspended                                                                                                                           |
| 000Ch                 | RW     | IR_SUSPEND       | IR Sensor Discontinuous Turned ON. Controlled by GPIO3                                                                                                                                  |
| <b>IrDA Registers</b> |        |                  |                                                                                                                                                                                         |
| FC00~FC7F             | -      | IR_RX_BUFF       | Normal Mode: The 128-byte buffer is for receiving RLC encoded waveform data<br>Suspend Mode: Used to save original power key RLC encoded data for comparing with received waveform data |
| FD00h                 | -      | IR_RX_IE         | Interrupt Enable Register. Not Available in Suspend Mode                                                                                                                                |
| FD01h                 | -      | IR_RX_IF         | Interrupt Flag Register. Not Available in Suspend Mode                                                                                                                                  |
| FD02h                 | -      | IR_RX_CTRL       | IR Receive Control Register                                                                                                                                                             |
| FD03h                 | -      | IR_RX_CONFIG     | IR Receive Configure Register                                                                                                                                                           |
| FD04h                 | -      | IR_MAX_DURATION0 | Max Time Duration Configure Register                                                                                                                                                    |

| Address Offset                         | Access | Name                   | Description                                              |
|----------------------------------------|--------|------------------------|----------------------------------------------------------|
| FD05h                                  | -      | IR_MAX_DURATION1       | Max Time Duration Configuration Register                 |
| FD06h                                  | -      | IR_IDLE_LEN0           | Idle Length Configuration Register                       |
| FD07h                                  | -      | IR_IDLE_LEN1           | Idle Length Configuration Register                       |
| FD08h                                  | -      | IR_GLITCH_LEN          | Glitch Length Configuration Register                     |
| FD09h                                  | -      | IR_RX_BUFFER_CTRL      | IR RX Buffer Control Register                            |
| FD0Ah                                  | -      | IR_RX_BUFFER_DATA      | IR Buffer Data for MCU Access                            |
| FD0Bh                                  | -      | IR_RX_BC               | Frame RX Byte Counter Register                           |
| FD0Ch                                  | -      | IR_RX_CLK              | Frame RX Byte Counter Register. Not Available in Suspend |
| FD0Dh                                  | -      | IR_RX_C_COUNT_L        | IR Received Carrier Count Register                       |
| FD0Eh                                  | -      | IR_RX_C_COUNT_H        | IR Received Carrier Count Register                       |
| FD0Fh                                  | -      | -                      | Reserved                                                 |
| FD10h                                  | -      | IR_SUSPEND_CTRL        | Suspend Control Register                                 |
| FD11h                                  | -      | IR_Err_Tolerance_CTRL  | IR Error Tolerance Control Register                      |
| FD12h                                  | -      | IR_UNIT_LEN            | 1T Unit Length Register                                  |
| FD13h                                  | -      | IR_ERR_Tolerance_LEN   | High Level Unit Negative Tolerance Length Register       |
| FD14h                                  | -      | IR_MAX_H_Tolerance_LEN | High Level Max Tolerance Length Register                 |
| FD15h                                  | -      | IR_MAX_L_Tolerance_LEN | Low Level Max Tolerance Length Register                  |
| FD16h                                  | -      | IR_MASK_CTRL           | Mask Control Register                                    |
| FD17h                                  | -      | IR_MASK_DATA           | Mask Data Register                                       |
| FD18h                                  | -      | IR_RESUME_MASK_ADDR    | IR Resume Mask Address Register                          |
| FD19h                                  | -      | IR_RESUME_MASK_T_LEN   | IR Resume Mask Length Register                           |
| <b>I<sup>2</sup>C Master Registers</b> |        |                        |                                                          |
| 0040h                                  | RW     | I2CCR                  | I <sup>2</sup> C Clock Register                          |
| 0044h                                  | RW     | I2CMCR                 | I <sup>2</sup> C Master Control Register                 |
| 0048h                                  | RW     | I2CMSTR                | I <sup>2</sup> C Master SCL Timing Register              |
| 004Ch                                  | RW     | I2CMSR                 | I <sup>2</sup> C Master Status Register                  |
| 0050h                                  | RW     | I2CMFR                 | I <sup>2</sup> C Master FIFO Register.                   |

## 10.1. Demodulator Control Register (DEMOD\_CTL, 0000h)

**Table 15. Demodulator Control Register (DEMOD\_CTL, 0000h)**

| Bits | Access | Reset | Description                                                                                |
|------|--------|-------|--------------------------------------------------------------------------------------------|
| 7    | RW     | 0     | Demodulator PLL Enable. Set to 1 to enable demodulator PLL, and to 0 to disable            |
| 6    | RW     | 0     | Demodulator ADC_I Enable. Set to 1 to enable ADC operation and to 0 to disable             |
| 5    | RW     | 1     | Demodulator Hardware Reset. Set to 0 to activate hardware reset, and to 1 to release reset |
| 4    | -      | -     | Reserved                                                                                   |
| 3    | RW     | 0     | Demodulator ADC_Q Enable. Set 1 to enable ADC operation and 0 to disable                   |
| 2:0  | -      | -     | Reserved                                                                                   |

## 10.2. GPIO Related Registers (0001h~0008h)

The following registers are used to control GPIO 0~7. The default functions of these 8 pins are:

1. GPIO [0]: Output for VDD1 power control. Default value 1 to turn off power.
2. GPIO [1]: Input for power-on latch to select clock source. Input value depends on the crystal on board; default 0 for 28.8MHz.
3. GPIO [2]: Input for external I<sup>2</sup>C mode, internal pull-down. This pin is used for LED control after 8051 firmware runs, and will set to 0 to turn off the LED, or 1 to turn it on.
4. GPIO [3]: Input for USB remote wakeup. Input value 0 is to activate remote wakeup.  
Output for tuner power control. Default value 1 to turn off power.
5. GPIO [4]: Output for antenna power control. Default value 0 to turn off power.
6. GPIO [5]: Input for power-on latch to select clock source, input value depends on the crystal on board. Default 0 for 28.8MHz.
7. GPIO [6]: Reserved.
8. GPIO [7]: Reserved.

### 10.2.1. GPIO Output Value Register (GPO, 0001h)

**Table 16. GPIO Output Value Register (GPO, 0001h)**

| Bits | Access | Reset | Description                                                              |
|------|--------|-------|--------------------------------------------------------------------------|
| 7    | RW     | 0     | Output Value of GPIO 7. Valid only when GPIO 7 is defined as output pin. |
| 6    | RW     | 0     | Output Value of GPIO 6. Valid only when GPIO 6 is defined as output pin. |
| 5    | RW     | 0     | Output Value of GPIO 5. Valid only when GPIO 5 is defined as output pin. |
| 4    | RW     | 1     | Output Value of GPIO 4. Valid only when GPIO 4 is defined as output pin. |
| 3    | RW     | 1     | Output Value of GPIO 3. Valid only when GPIO 3 is defined as output pin. |
| 2    | RW     | 0     | Output Value of GPIO 2. Valid only when GPIO 2 is defined as output pin. |
| 1    | RW     | 0     | Output Value of GPIO 1. Valid only when GPIO 1 is defined as output pin. |
| 0    | RW     | 0     | Output Value of GPIO 0. Valid only when GPIO 0 is defined as output pin. |

### 10.2.2. GPIO Input Value Register (GPI, 0002h)

**Table 17. GPIO Input Value Register (GPI, 0002h)**

| Bits | Access | Reset | Description                                                            |
|------|--------|-------|------------------------------------------------------------------------|
| 7    | R      | -     | Input Value of GPIO 7. Valid only when GPIO 7 is defined as input pin. |
| 6    | R      | -     | Input Value of GPIO 6. Valid only when GPIO 6 is defined as input pin. |
| 5    | R      | -     | Input Value of GPIO 5. Valid only when GPIO 5 is defined as input pin. |
| 4    | R      | -     | Input Value of GPIO 4. Valid only when GPIO 4 is defined as input pin. |
| 3    | R      | -     | Input Value of GPIO 3. Valid only when GPIO 3 is defined as input pin. |
| 2    | R      | -     | Input Value of GPIO 2. Valid only when GPIO 2 is defined as input pin. |
| 1    | R      | -     | Input Value of GPIO 1. Valid only when GPIO 1 is defined as input pin. |
| 0    | R      | -     | Input Value of GPIO 0. Valid only when GPIO 0 is defined as input pin. |

### 10.2.3. GPIO Output Enable Register (GPOE, 0003h)

**Table 18. GPIO Output Enable Register (GPOE, 0003h)**

| Bits | Access | Reset | Description                                                                                                                                       |
|------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 7    | RW     | 0     | Output Enable for GPIO 7. Valid only when GPIO 7 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 6    | RW     | 0     | Output Enable for GPIO 6. Valid only when GPIO 6 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 5    | RW     | 0     | Output Enable for GPIO 5. Valid only when GPIO 5 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 4    | RW     | 1     | Output Enable for GPIO 4. Valid only when GPIO 4 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 3    | RW     | 1     | Output Enable for GPIO 3. Valid only when GPIO 3 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 2    | RW     | 0     | Output Enable for GPIO 2. Valid only when GPIO 2 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 1    | RW     | 0     | Output Enable for GPIO 1. Valid only when GPIO 1 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |
| 0    | RW     | 1     | Output Enable for GPIO 0. Valid only when GPIO 0 is defined as output pin.<br>1: Output enable                      0: Output disable (tri-state) |

### 10.2.4. GPIO Direction Control Register (GPD, 0004h)

**Table 19. GPIO Direction Control Register (GPD, 0004h)**

| Bits | Access | Reset | Description                                                            |
|------|--------|-------|------------------------------------------------------------------------|
| 7    | RW     | 0     | Direction Control of GPIO 7<br>1: Input                      0: Output |
| 6    | RW     | 0     | Direction Control of GPIO 6<br>1: Input                      0: Output |
| 5    | RW     | 0     | Direction Control of GPIO 5<br>1: Input                      0: Output |
| 4    | RW     | 0     | Direction Control of GPIO 4<br>1: Input                      0: Output |
| 3    | RW     | 1     | Direction Control of GPIO 3<br>1: Input                      0: Output |

| <b>Bits</b> | <b>Access</b> | <b>Reset</b> | <b>Description</b>                                                     |
|-------------|---------------|--------------|------------------------------------------------------------------------|
| 2           | RW            | 1            | Direction Control of GPIO 2<br>1: Input                      0: Output |
| 1           | RW            | 1            | Direction Control of GPIO 1<br>1: Input                      0: Output |
| 0           | RW            | 0            | Direction Control of GPIO 0<br>1: Input                      0: Output |

### 10.2.5. PAD Configuration Register for GPIO0~3 (GP\_CFG0, 0007h)

**Table 20. PAD Configuration Register for GPIO0~3 (GP\_CFG0, 0007h)**

| Bits | Access | Reset | Description                                                            |
|------|--------|-------|------------------------------------------------------------------------|
| 7:6  | RW     | 2h    | GP_PAD3. PAD configuration as internal pull-up or pull-down for GPIO3. |
| 5:4  | RW     | 1h    | GP_PAD2. PAD configuration as internal pull-up or pull-down for GPIO2. |
| 3:2  | RW     | 1h    | GP_PAD1. PAD configuration as internal pull-up or pull-down for GPIO1. |
| 1:0  | RW     | 2h    | GP_PAD0. PAD configuration as internal pull-up or pull-down for GPIO0. |

### 10.2.6. PAD Configuration Register for GPIO4 (GP\_CFG1, 0008h)

**Table 21. PAD Configuration Register for GPIO4 (GP\_CFG1, 0008h)**

| Bits | Access | Reset | Description                                                            |
|------|--------|-------|------------------------------------------------------------------------|
| 7:6  | RW     | 1h    | GP_PAD7. PAD configuration as internal pull-up or pull-down for GPIO7. |
| 5:4  | RW     | 1h    | GP_PAD6. PAD configuration as internal pull-up or pull-down for GPIO6. |
| 3:2  | RW     | 1h    | GP_PAD5. PAD configuration as internal pull-up or pull-down for GPIO5. |
| 1:0  | RW     | 1h    | GP_PAD4. PAD configuration as internal pull-up or pull-down for GPIO4. |

*Note: PAD pull-up or pull-down (PU:PD) configuration is:*

1.  $[0:0]$  – Normal No pull-up or pull-down.
2.  $[0:1]$  –  $75k\Omega$  resistor pull-down.
3.  $[1:0]$  –  $75k\Omega$  resistor pull-up.

### 10.3. I<sup>2</sup>C Master Control Registers (0040h-0053h)

#### 10.3.1. I<sup>2</sup>C Clock Register (I2CCR, 0040h-0043h)

**Table 22. I<sup>2</sup>C Clock Register (I2CCR, 0040h-0043h)**

| Bits | Access | Reset | Description                                                                                                                                                                          |
|------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | -      | -     | Reserved                                                                                                                                                                             |
| 5:0  | RW     | 13h   | FD10. Frequency 10M Divisor and 0 are forbidden. 10M=Bus clock/(FD10+1).<br>When powered on, software must write FD10 to let the I <sup>2</sup> C controller generate a 10MHz clock. |

#### 10.3.2. I<sup>2</sup>C Master Control Register (I2CMCR, 0044h-0047h)

**Table 23. I<sup>2</sup>C Master Control Register (I2CMCR, 0044h-0047h)**

| Bits  | Access | Reset | Description                                                                                                                                                                                                                                                            |
|-------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RW     | 0     | IMUR. I <sup>2</sup> C Master Unit Reset<br>0: Normal<br>1: Reset the I <sup>2</sup> C Unit (only resets hardware FSM). This bit will self-clear to Zero after reset complete                                                                                          |
| 30    | RW     | 0     | CS. Command Start<br>0: Stop. After completing a whole transaction, it returns to Zero<br>1: Start                                                                                                                                                                     |
| 29:25 | RW     | 0     | RWL. Read/Write Data Length for Related Commands<br>Does not include the slave address byte in the FIFO register.<br>When accessed, the controller will parse the byte following the last start (or Sr) byte to find the command type.<br>0: 1 byte ..... 17: 24 bytes |
| 24    | RW     | 1     | TOR. Time-Out Register Enable<br>If TOR is required, the I <sup>2</sup> C rate must be constrained within 25kbps~400kbps.<br>This constraint is due to the time-out register bit.                                                                                      |

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### 10.3.3. I<sup>2</sup>C Master SCL Timing Register (I2CMSTR, 0048h-004Bh)

**Table 24. I<sup>2</sup>C Master SCL Timing Register (I2CMSTR, 0048h-004Bh)**

| Bits  | Access | Reset | Description                                                                                                                                                                                      |
|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | -      | -     | Reserved                                                                                                                                                                                         |
| 30:28 | RW     | 0     | I2CMD. I <sup>2</sup> C Master De-Bounce<br>0: Sample rate=(bus clk / (FD10+1))<br>1: Sample rate=(bus clk / (FD10+1)) / 2<br>.....<br>7: Sample rate= (bus clk / (FD10+1)) / 8                  |
| 27:20 | RW     | 9h    | STA_SU_PC. STA Setup Time Period Count<br>In repeat start, the setup time of SCL must match the I <sup>2</sup> C spec.                                                                           |
| 19:16 | RW     | 3h    | FTPC. Fall Time Period Count<br>If the value of (Bus clock/FD10) does not approximate 10MHz, FTPC can make the fall time of SCL more than 300ns.                                                 |
| 15:8  | RW     | 9h    | SHPC. SCL High Period Counter (SCL High Period=100ns*SHPC)<br>SHPC must include rising time in the I <sup>2</sup> C.<br>The I <sup>2</sup> C specification requires SHPC to include rising time. |
| 7:0   | RW     | 10h   | SLPC. SCL Low Period Counter (SCL Low Period=100ns*SLPC)<br>The I <sup>2</sup> C specification requires SLPC to include falling time.                                                            |

### 10.3.4. I<sup>2</sup>C Master Status Register (I2CMSR, 004Ch-004Fh)

**Table 25. I<sup>2</sup>C Master Status Register (I2CMSR, 004Ch-004Fh)**

| Bits | Access | Reset | Description                                                                                                                                                                                              |
|------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | -      | -     | Reserved                                                                                                                                                                                                 |
| 2    | RW     | 0     | TEIF. Transaction Error Interrupt Flag<br>When a master transmit/receive fault or time-out occurs, the I <sup>2</sup> C controller will lift the flag up and return the bus to idle. Write '1' to clear. |
| 1    | RW     | 0     | MRCIF. Master Receive Complete Interrupt Flag. Write '1' to clear.                                                                                                                                       |
| 0    | RW     | 0     | MTCIF. Master Transmit Complete Interrupt Flag. Write '1' to clear.                                                                                                                                      |

### 10.3.5. I<sup>2</sup>C Master FIFO Register (I2CMFR, 0050h-0053h)

**Table 26. I<sup>2</sup>C Master FIFO Register (I2CMFR, 0050h-0053h)**

| Bits | Access | Reset | Description                                |
|------|--------|-------|--------------------------------------------|
| 31:8 | -      | -     | Reserved                                   |
| 7:0  | RW     | 0     | TDD. Target Device Data. Read for receive. |

## 11. Register Descriptions (USB Interface)

### 11.1. Introduction

The RTL2832U transfers transport stream data from the demodulation module to the host via an embedded high-speed USB 2.0 interface (compatible with USB 1.1). Two endpoints are supplied. One is the control pipe and the other is the data pipe for TS transfer. The user controls the device by sending standard request commands listed in the USB 2.0 Specification, Chapter 9. The host driver also needs to read and write the device's registers by sending vendor commands (11.1). The data pipe can be configured to BULK mode or ISO mode.

To reduce power consumption, the RTL2832U can enter a low-power suspend state, and has a remote wakeup capability via IrDA. It can resume from S1, S3, or selective suspend state if the remote wakeup function is permitted on the host.

### 11.2. Vendor Commands

**Table 27. Vendor Commands**

| Command                               | bmRequestType<br>(1 Byte) | bRequest<br>(1 Byte) | wValue<br>(2 Bytes)      | wIndex<br>(2 Bytes) | wLength<br>(2 Bytes)             |
|---------------------------------------|---------------------------|----------------------|--------------------------|---------------------|----------------------------------|
| GetDemodRegPage0<br>~GetDemodRegPage4 | 0xC0                      | x                    | Reg's offset in page0~4  | 0x0000~<br>0x0004   | Length of registers<br>to access |
| SetDemodRegPage0<br>~SetDemodRegPage4 | 0x40                      | x                    | Reg's offset in page0~4  | 0x0010~<br>0x0014   | Length of registers<br>to access |
| GetUSBReg                             | 0xC0                      | x                    | (BaseAdd)<<8 + OffsetAdd | 0x0100              | Length of registers<br>to access |

| Command    | bmRequestType<br>(1 Byte) | bRequest<br>(1 Byte) | wValue<br>(2 Bytes)                                         | wIndex<br>(2 Bytes) | wLength<br>(2 Bytes)          |
|------------|---------------------------|----------------------|-------------------------------------------------------------|---------------------|-------------------------------|
| SetUSBReg  | 0x40                      | x                    | (BaseAdd)<<8 + OffsetAdd                                    | 0x0110              | Length of registers to access |
| GetSysReg  | 0xC0                      | x                    | (BaseAdd)<<8 + OffsetAdd                                    | 0x0200              | Length of registers to access |
| SetSysReg  | 0x40                      | x                    | (BaseAdd)<<8 + OffsetAdd                                    | 0x0210              | Length of registers to access |
| GetTunReg  | 0xC0                      | x                    | (OffsetAdd)<<8+ IICAdd                                      | 0x0300              | Length of registers to access |
| SetTunReg  | 0x40                      | x                    | (OffsetAdd)<<8+ IICAdd                                      | 0x0310              | Length of registers to access |
| GetROMCode | 0xC0                      | x                    | Rom Code Address                                            | 0x0400              | Size of ROM Code              |
| GetSTDI2C  | 0xC0                      | x                    | I <sup>2</sup> C Device Address/<br>Device register address | 0x0600              | Length of registers to access |
| SetSTDI2C  | 0x40                      | x                    | I <sup>2</sup> C Device Address/<br>Device register address | 0x0610              | Length of registers to access |

Note1: Demod registers are organized in 5 pages (page0~page4). 'wIndex' indicates the page's number.

Note2: Before accessing the tuner, the 7<sup>th</sup> bit of the first byte of the demodulator's page1 should be set to 1 (IIC\_repeat bit).

**Table 28. Definition of 'wIndex'**

| Nibble      | [3] | [2]                               |     |        |       |          |    | [1]    |     | [0]                                        |
|-------------|-----|-----------------------------------|-----|--------|-------|----------|----|--------|-----|--------------------------------------------|
| Description | x   | Block                             |     |        |       |          |    | Access |     | Page (true only as [2]=0, for demodulator) |
|             | 0   | 0                                 | 1   | 2      | 3     | 4        | 5  | 0      | 1   | 0 – 4                                      |
|             |     | Demodulator                       | USB | System | Tuner | ROM Code | IR | Get    | Set | Page number                                |
|             |     | 6                                 | 7   | 8      | 9     | A        | B  |        |     |                                            |
|             |     | Standard I <sup>2</sup> C Command | x   | x      | x     | x        | x  |        |     |                                            |

Note: To access the tuner, the command is issued within the DATA stage, ignoring the 'wValue' field value. The command depends on the tuner used.

### 11.3. SIE Control Register

The registers for USB SIE is defined in Table 29, including SIE control registers, endpoint registers, debugging registers, and DMA control registers. The address is defined by an offset value with base address 0x2000.

**Table 29. SIE Control Register**

| Address Offset | Name             | Description                         |
|----------------|------------------|-------------------------------------|
| 0000h          | USB_SYSCTL       | USB System Control Register         |
| 0004h~0010h    | -                | Reserved                            |
| 0008h          | -                | Reserved                            |
| 000Ch          | -                | Reserved                            |
| 0010h          | -                | Reserved                            |
| 0014h          | -                | Reserved                            |
| 0018h          | -                | Reserved                            |
| 001C~0140h     | -                | Reserved                            |
| 0144h          | USB_EPA_CFG      | Endpoint A Configure Register       |
| 0148h          | USB_EPA_CTL      | Endpoint A Control Register         |
| 014C~0154h     | -                | Reserved                            |
| 0158h          | USB_EPA_MAXPKT   | Endpoint A Max Packet Size Register |
| 015Ch          | -                | Reserved                            |
| 0160h          | USB_EPA_FIFO_CFG | Endpoint A FIFO Configure Register  |
| 0164h~0FFFh    | -                | Reserved                            |

## 11.4. USB System Control Register (USB\_SYSCTL, 0000h)

**Table 30. USB System Control Register (USB\_SYSCTL, 0000h)**

| Bits  | Access | Reset | Description                                                                                                                                                                 |
|-------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | -      | -     | Reserved                                                                                                                                                                    |
| 10    | RW     | 0     | SIE Reset<br>1: Switch to reset state                      0: Switch to normal state                                                                                        |
| 9:4   | -      | -     | Reserved                                                                                                                                                                    |
| 3     | RW     | 0     | Full Packet Mode<br>When set to 1, SIE will send maximum packet size packets only. When data in EPA FIFO is less than the maximum packet size, SIE will NAK the IN request. |
| 2:1   | -      | -     | Reserved                                                                                                                                                                    |
| 0     | RW     | 1     | DMA Control<br>1: Enable DMA                                      0: Disable DMA                                                                                            |

### 11.4.1. Endpoint A Configuration Register (USB\_EPA\_CFG, 0144h)

**Table 31. Endpoint A Configuration Register (USB\_EPA\_CFG, 0144h)**

| Bits  | Access | Reset | Description                                                                                                                                                                                                                            |
|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | -      | -     | Reserved                                                                                                                                                                                                                               |
| 9:8   | RW     | 0     | Isochronous Mode<br>Specifies the number of additional transaction opportunities per microframe (same definition as wMaxPacketSize[12:11] in standard Endpoint Descriptor).<br>Must be set to 00 (means 1 transaction per microframe). |
| 7     | RW     | 0     | Endpoint Enable<br>0: Disable Endpoint A                                      1: Enable Endpoint A.                                                                                                                                    |
| 6:5   | RW     | 10b   | Endpoint Transfer Type<br>00: Control (only EP0 can be for control)                      01: Isochronous<br>10: Bulk                                                                                      11: Interrupt                |
| 4     | R      | -     | Endpoint Transfer Direction<br>0: OUT. Host-to-device                                                                                      1: IN. Device-to-host                                                                       |
| 3:0   | RW     | 0     | Endpoint Number                                                                                                                                                                                                                        |

### 11.4.2. Endpoint A Control Register (USB\_EPA\_CTL, 0148h)

**Table 32. Endpoint A Control Register (USB\_EPA\_CTL, 0148h)**

| Bits  | Access | Reset | Description                                                           |
|-------|--------|-------|-----------------------------------------------------------------------|
| 31:10 | -      | -     | Reserved                                                              |
| 9     | RW     | 0     | FIFO Reset. Reset EPA FIFO                                            |
| 8:6   | -      | -     | Reserved                                                              |
| 5     | W      | 0     | FIFO Flush. Write 1 to flush the oldest TS packet (a 188 bytes block) |
| 4     | RW     | 0     | Stall Endpoint. Write 1 to stall                                      |
| 3:1   | -      | -     | Reserved                                                              |
| 0     | W      | 0     | FIFO Valid. Write 1 to validate the TS packet (a 188 bytes block)     |

### 11.4.3. Endpoint A Max Packet Size Register (USB\_EPA\_MAXPKT, 0158h)

**Table 33. Endpoint A Max Packet Size Register (USB\_EPA\_MAXPKT, 0158h)**

| Bits  | Access | Reset | Description                                                                  |
|-------|--------|-------|------------------------------------------------------------------------------|
| 31:11 | -      | -     | Reserved                                                                     |
| 10:0  | RW     | 40h   | EPA Max Packet Size<br>Defines the max packet size (in bytes) of endpoint A. |

### 11.4.4. Endpoint A FIFO Configuration Register (USB\_EPA\_FIFO\_CFG, 0160h)

**Table 34. Endpoint A FIFO Configuration Register**

| Bits  | Access | Reset    | Description                                                                              |
|-------|--------|----------|------------------------------------------------------------------------------------------|
| 31:24 | RW     | 0        | BLK_DROP_COUNTER<br>Counts blocks dropped (each is 188 bytes) due to full FIFO.          |
| 23:4  | -      | -        | Reserved.                                                                                |
| 3:0   | RW     | Ah (10d) | EPA FIFO Size<br>Configures EPA FIFO size, in 188-byte blocks. Valid data range is 1~10. |

## 12. Characteristics

### 12.1. Absolute Maximum Ratings

**Table 35. Absolute Maximum Ratings**

| Description                                | Minimum | Maximum | Unit |
|--------------------------------------------|---------|---------|------|
| Supply Voltage (VDD3, VDDA33)              | -0.5    | 4       | V    |
| Supply Voltage (VDD1, VDDA, UVDDA, VDDPLL) | -0.5    | 1.35    | V    |
| Storage Temperature                        | -55     | +125    | °C   |

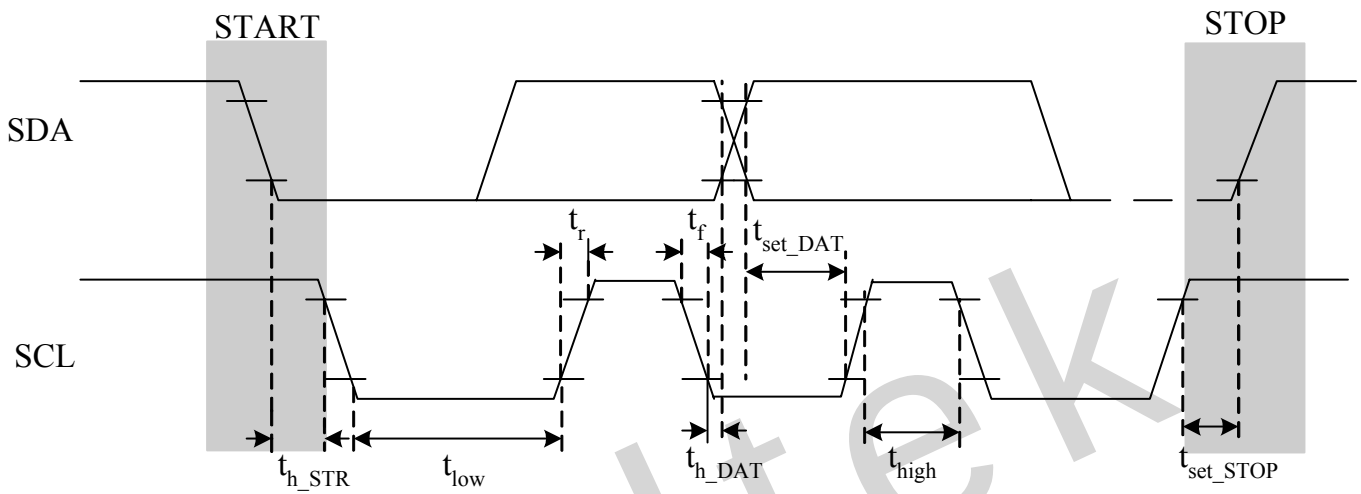
### 12.2. DC Characteristics

**Table 36. DC Characteristics**

| Symbol                            | Parameter                                  | Conditions            | Minimum  | Typical | Maximum  | Unit |
|-----------------------------------|--------------------------------------------|-----------------------|----------|---------|----------|------|
| VDD3, VDDA33                      | 3.3V Supply Voltage                        | -                     | 3.0      | 3.3     | 3.6      | V    |
| VDDPLL, VDDA, UVDDA               | 1.2V Supply Voltage                        | -                     | 1.1      | 1.2     | 1.35     | V    |
| VDD1                              | 1.2V Supply Voltage                        | -                     | 1.1      | 1.2     | 1.35     | V    |
| V <sub>oh</sub>                   | Minimum High Level Output Voltage          | I <sub>oh</sub> =-8mA | 0.9*VDD3 | -       | VDD3     | V    |
| V <sub>ol</sub>                   | Maximum Low Level Output Voltage           | I <sub>ol</sub> =-8mA | -        | -       | 0.1*VDD3 | V    |
| Icc33 (VDDA33, VDD3)              | Average Operating Supply Current from 3.3V | -                     | -        | 7       | -        | mA   |
| Icc12 (VDD1, VDDA, VDDPLL, UVDDA) | Average Operating Supply Current from 1.2V | -                     | -        | 202*    | -        | mA   |

\*: In case of 64QAM, Code rate=2/3, Guard Interval=1/4, Bandwidth=8MHz, bypass internal switching regulator.

### 12.3. AC Characteristics



**Figure 8. Two-Wire Interface Timing Diagram**

**Table 37. Two-Wire Interface Timing**

| Symbol          | Parameter                                                     | Min        | Max | Unit |
|-----------------|---------------------------------------------------------------|------------|-----|------|
| -               | SCL Clock Frequency                                           | 50         | 300 | kHz  |
| $t_{high}$      | High Period of SCL                                            | 600        | -   | ns   |
| $t_{low}$       | Low Period of SCL                                             | 600        | -   | ns   |
| $t_{h\_STR}$    | Hold Time of START                                            | 200        | -   | ns   |
| $t_{h\_DAT}$    | Hold Time of DATA                                             | 200        | -   | ns   |
| $t_{set\_STOP}$ | Setup Time of STOP                                            | 200        | -   | ns   |
| $t_{set\_DAT}$  | Setup Time of DATA                                            | 200        | -   | ns   |
| $t_r$           | Rise Time of SCL and SDA (with 4.7k ohm resistor pulled high) | (See Note) | -   | ns   |
| $t_f$           | Fall time of SCL and SDA                                      | (See Note) | -   | ns   |

Note: Depends on the external bus pull high resistor.

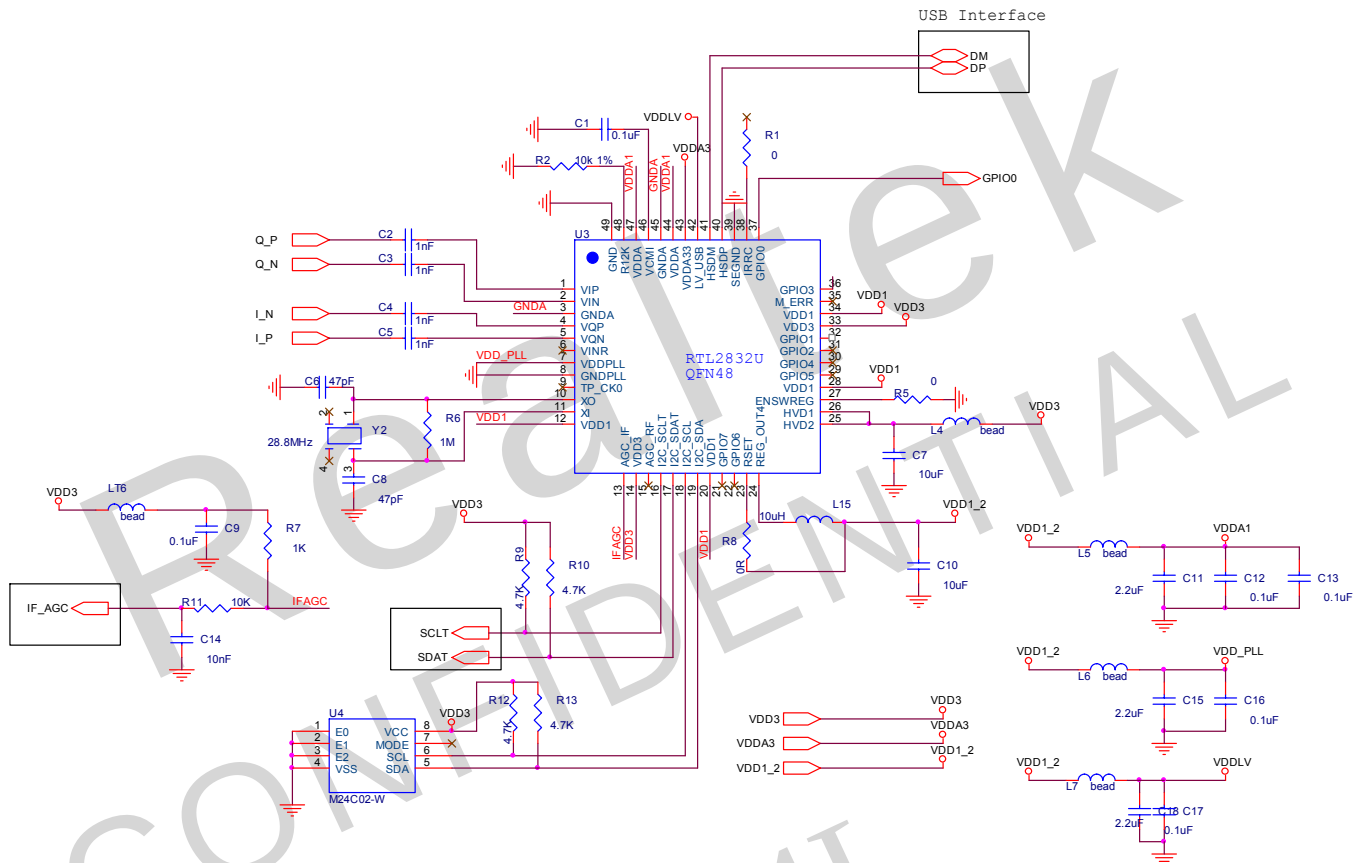
## 12.4. Crystal Conditions

**Table 38. Crystal Conditions**

| Description                                   | Minimum | Typical | Maximum | Unit |
|-----------------------------------------------|---------|---------|---------|------|
| Crystal Reference Frequency, Fundamental Mode | -       | 28.8    | -       | MHz  |
| Stability                                     | -30     | -       | +30     | ppm  |
| Tolerance                                     | -30     | -       | +30     | ppm  |
| Duty Cycle                                    | 40      | -       | 60      | %    |
| Load Capacitance                              | -       | 20      | -       | pF   |
| C0 (Shunt Capacitance)                        | -       | -       | 5pF     | pF   |
| ESR (Equivalent Series Resistance)            | -       | -       | 30      | ohm  |

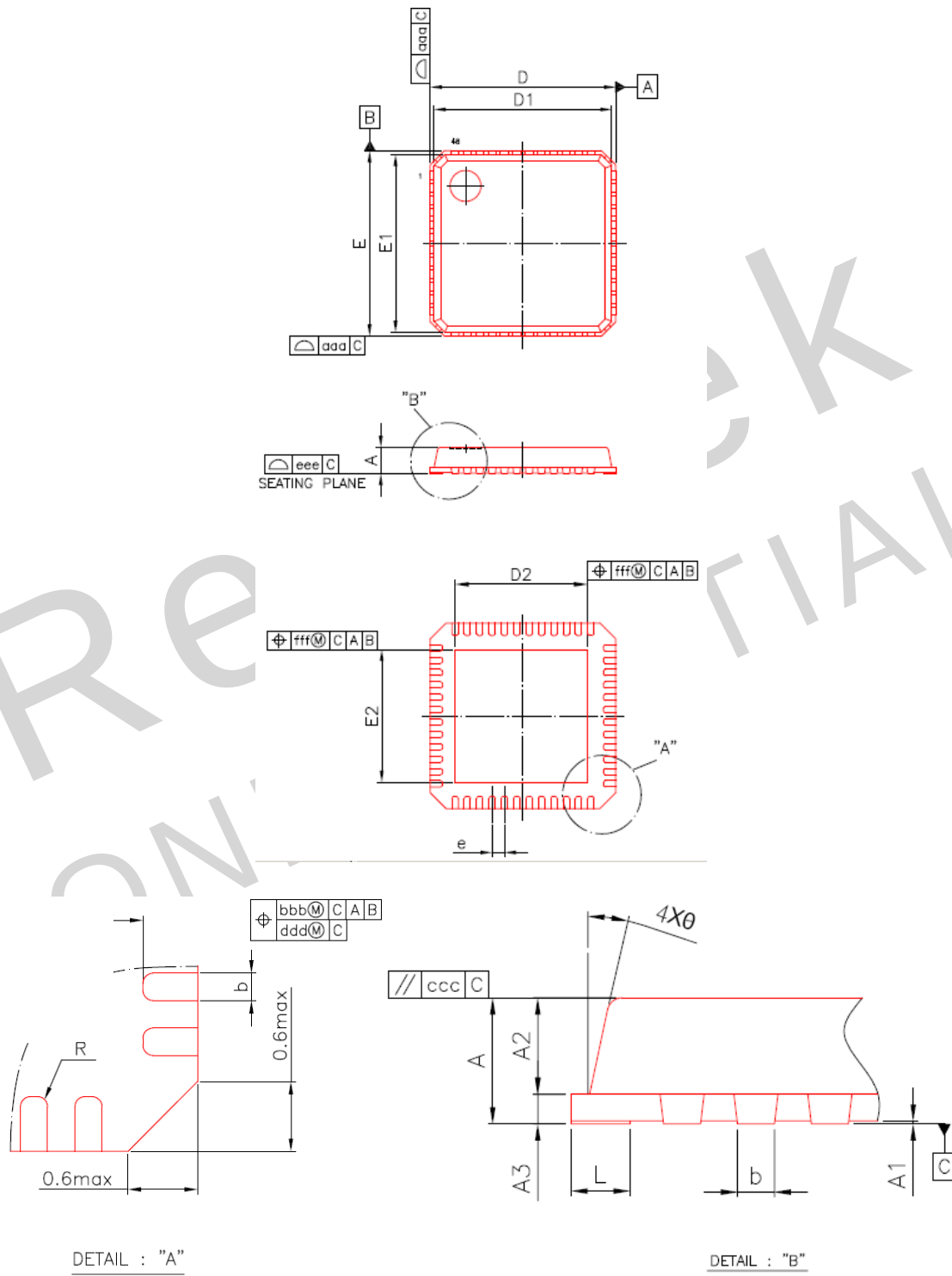
## 13. Application Circuits

Designers are suggested to contact Realtek to get the latest application circuits. To get the best compatibility in hardware design and software driver, any modifications of application circuits should be confirmed by us. Realtek may update the latest application circuits onto our website ([www.realtek.com](http://www.realtek.com)) without modifying this datasheet.



**Figure 9. Application Circuits**

## 14. Mechanical Dimensions



## 14.1. Mechanical Dimensions Notes

| Symbol                         | Dimension in mm |      |      | Dimension in inch |       |       |
|--------------------------------|-----------------|------|------|-------------------|-------|-------|
|                                | Min             | Nom  | Max  | Min               | Nom   | Max   |
| A                              | 0.75            | 0.85 | 1.00 | 0.030             | 0.034 | 0.039 |
| A <sub>1</sub>                 | 0.00            | 0.02 | 0.05 | 0.000             | 0.001 | 0.002 |
| A <sub>2</sub>                 | 0.55            | 0.65 | 0.80 | 0.022             | 0.026 | 0.032 |
| A <sub>3</sub>                 | 0.20REF         |      |      | 0.008REF          |       |       |
| b                              | 0.15            | 0.20 | 0.25 | 0.006             | 0.008 | 0.010 |
| D/E                            | 6.00BSC         |      |      | 0.236BSC          |       |       |
| D <sub>1</sub> /E <sub>1</sub> | 5.75BSC         |      |      | 0.226BSC          |       |       |
| D <sub>2</sub> /E <sub>2</sub> | 4.05            | 4.30 | 4.55 | 0.159             | 0.169 | 0.179 |
| e                              | 0.40BSC         |      |      | 0.016BSC          |       |       |
| L                              | 0.30            | 0.40 | 0.50 | 0.012             | 0.016 | 0.020 |
| θ                              | 0°              | -    | 14°  | 0°                | -     | 14°   |
| aaa                            | -               | -    | 0.15 | -                 | -     | 0.006 |
| bbb                            | -               | -    | 0.10 | -                 | -     | 0.004 |
| ccc                            | -               | -    | 0.10 | -                 | -     | 0.004 |
| ddd                            | -               | -    | 0.05 | -                 | -     | 0.002 |
| eee                            | -               | -    | 0.08 | -                 | -     | 0.003 |
| fff                            | -               | -    | 0.10 | -                 | -     | 0.004 |

Notes 1: DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

Notes 2: CONTROLLING DIMENSION: MILLIMETER (mm).

Notes 3: REFERENCE DOCUMENT: JEDEC MO-220.

## 15. Ordering Information

**Table 39. Ordering Information**

| Part Number | Description                 | Status          |
|-------------|-----------------------------|-----------------|
| RTL2832U    | QFN-48 with 'Green' Package | Mass Production |

*Note: See page 4 for Green package and version identification.*

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